正基科技股份有限公司

AMPAK Technology Inc.

# AP12276_M2

## Evaluation Board User Manual

Address:
3F, No.15-1, Zhonghua Road, Hsinchu Industril Park, Hukou, Hsinchu,
Taiwan, 303035
Website: http://www.ampak.com.tw/

# Revision

| Revision | Date | Description | Revised By |
|---|---|---|---|
| 1.0 | 2024/ 10 / 07 | Initial released | Richard |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

# Contents

# 1. EVB Introduction

AP12276_M2 Evaluation board (EVB) likes as figure1. That is designed for IEEE802.11 a/b/g/n/ac/ax WLAN with integrated Bluetooth application. It is subject to provide a convenient environment for customer's verification on WiFi or Bluetooth function. There are many controller pins and reserved GPIO on Evaluation board which describes as below.

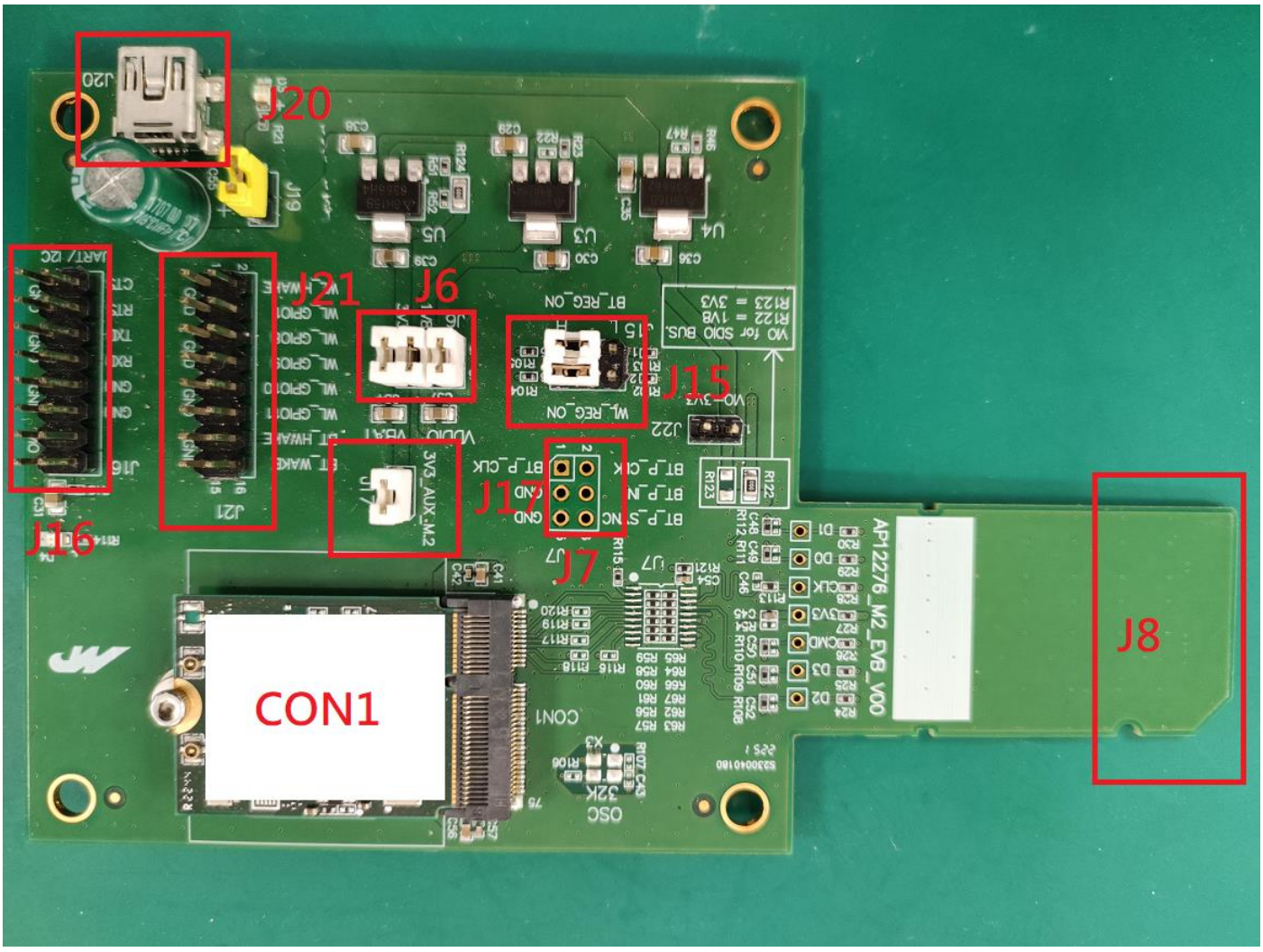



Figure1. Top view of AP12276_M2 EVB

**Interface highlights:**

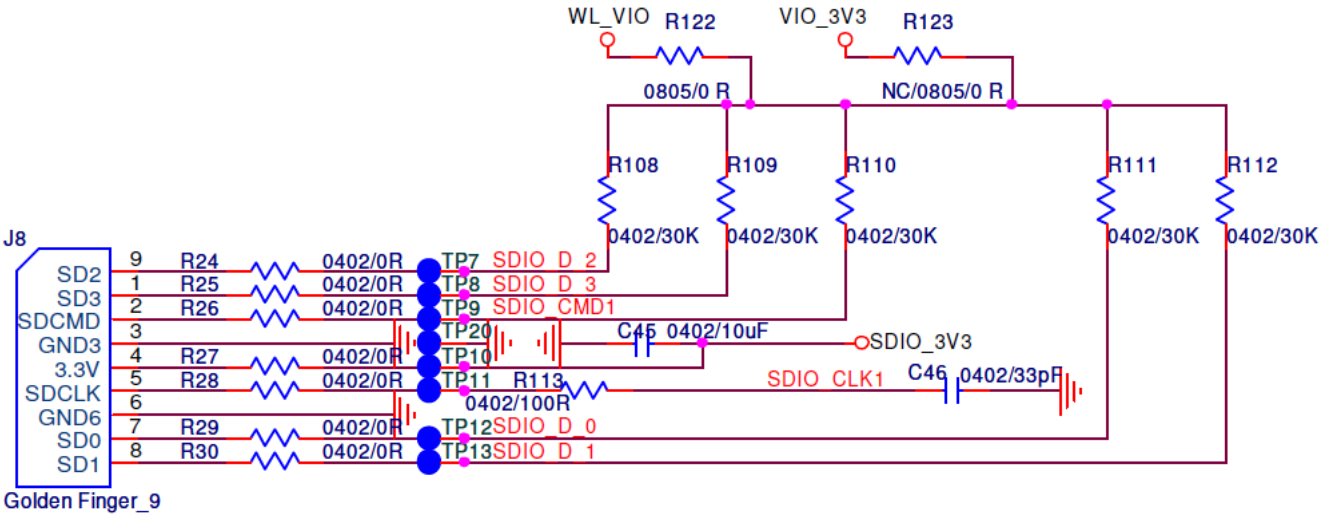
1. CON1: AP12276_M2 SIP module.
2. J16: UART interface connects with UART transport board for BT measuring
3. J15: Enable(H) or disable(L) Bluetooth, Wi-Fi function
4. J6: VBAT / WL_VIO / BT_VIO for main system I/O power path.
5. J20: 5V DC mini USB input connector.
6. J8: Standard SDIO interfaces for Wi-Fi performance measured.
7. J21: WL_HOST_WAKE/BT_HOST_WAKE/BT_DEV_WAKE/WL_GPIOs.
8. J7: BT_PCM interface.

9. J17: 3V3 jumper.

# 2. WiFi Function Verification Step

## 2.1 WiFi SDIO

Using external pull up resistors depends on the SDIO supply voltage. The resistance range is 30 KΩ~40 KΩ(for SDIO 3.0) on the four data lines and the CMD line as the following circuitry.




| | R122 | R123 | R108 | R109 | R110 | R111 | R112 | C46 |
|---|---|---|---|---|---|---|---|---|
| VIO=3.3V for Host (SDIO_2.0) | N/A | 0R | 200R | 200R | 1KR | 200R | 200R | 33pF |
| VIO=1.8V For Host (SDIO_2.0/3.0) | 0R | N/A | 30KR | 30KR | 30KR | 30KR | 30KR | N/A |

Figure2. Wi-Fi verification connection interface to Host SDIO as using SDIO2.0

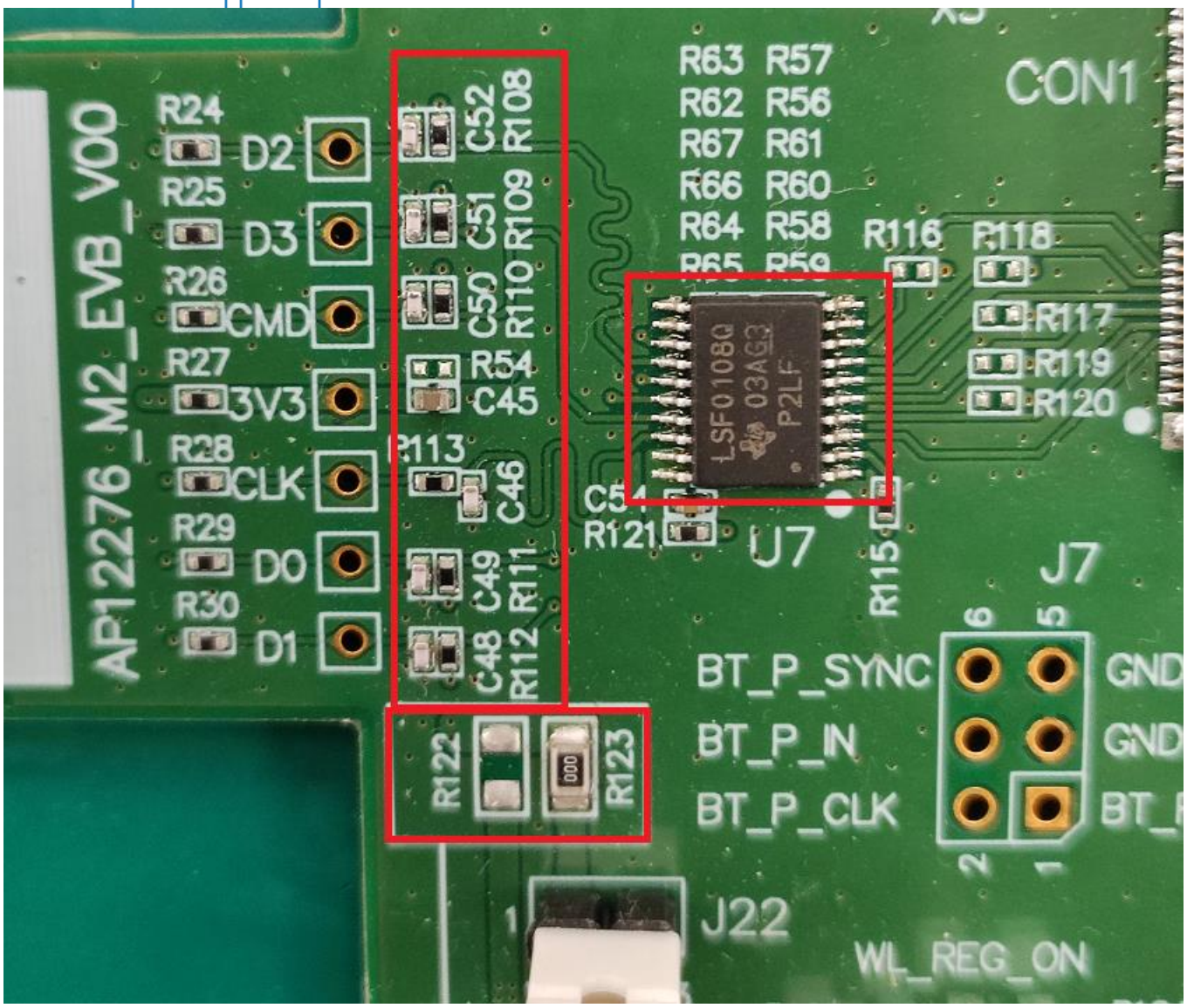



Figure3. EVB interface to HOST SDIO 2.0.

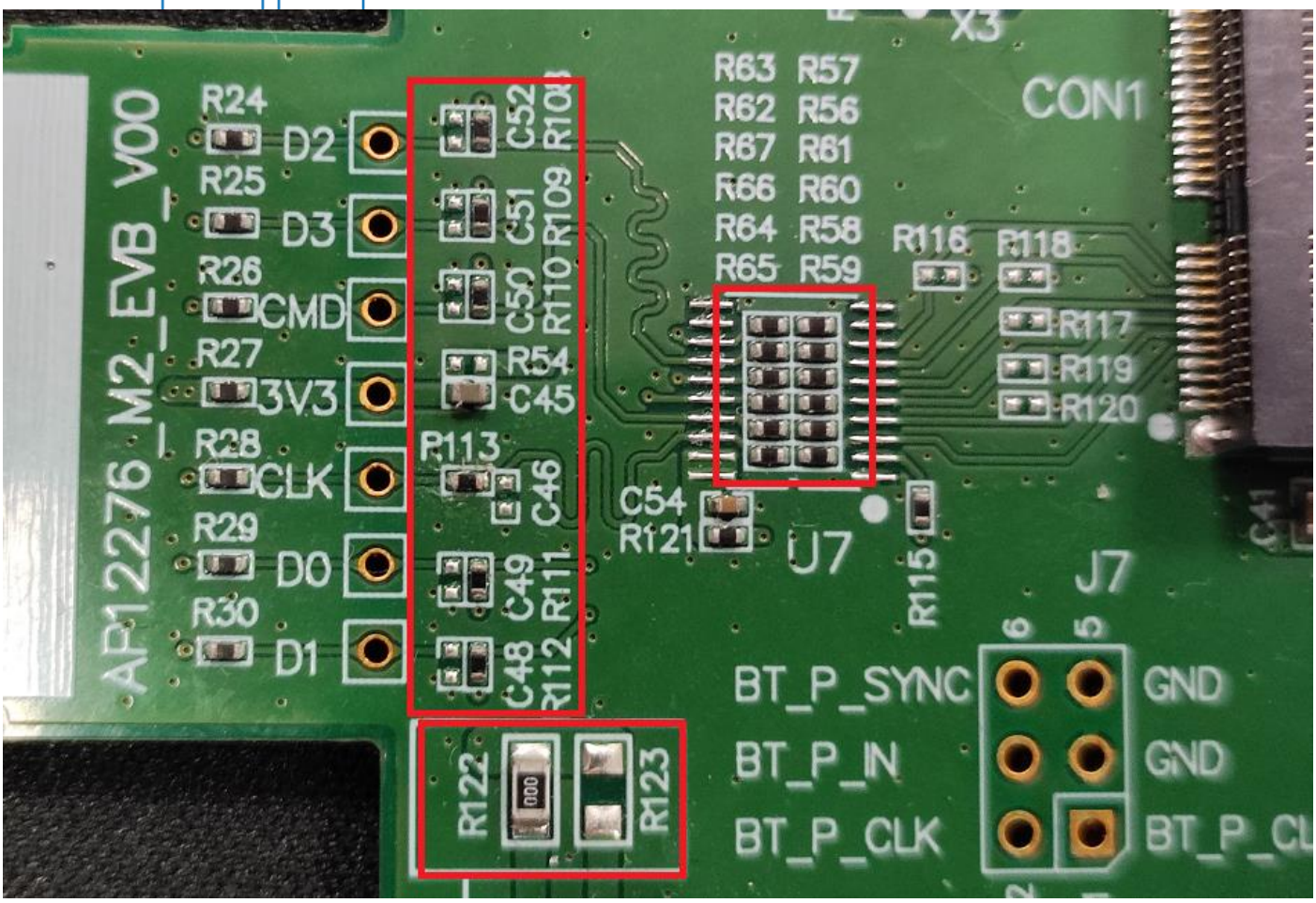



Figure4. EVB interface to HOST SDIO 3.0.

SDIO 2.0 Hardware Setup:

- ✧ Pull up voltage should be 3.3V, so make sure R123 is existed.
- ✧ U7 placed, R56/ R57/ R58/ R59/ R60/ R61/ R62/ R63/ R64/ R65/ R66/ R67 NOP.

SDIO 3.0 Hardware Setup:

- ✧ Pull up voltage should be 1.8V, so make sure R122 is existed.
- ✧ R56/ R57/ R58/ R59/ R60/ R61/ R62/ R63/ R64/ R65/ R66/ R67 placed, U7 NOP.

∗ U7 : TI – LSF0108QPWRQ1(Package : TSSOP)

## 2.2 Hardware Setup

- Refer to Figure2 SDIO pin definition connects the J8 interface of AP12276_M2 evaluation board to Host SDIO control interface.
- Using pull high resistors (R108, R109, R110, R111, R112) that resistance is 30Kohm for 1.8V or 3.3V VDDIO pull up voltage. (Pull high resistors are un-necessary if at verification phase.)
- Connects an external antenna at micro coaxial connector on the module.
- Note to the VDDIO voltage level should be the same with GPIO voltage level of Host CPU. (U7 is voltage level shift to 3.3V.)

## 2.3 WiFi Software Setup

- Please follow up software guideline of Ampak official released.

# 3. Bluetooth Function Verification Step

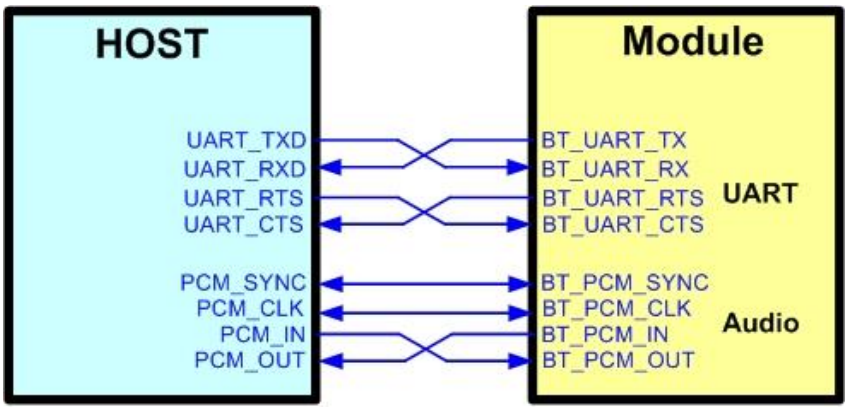



Figure5. Bluetooth verification connection interface to Host UART

Hardware Setup:

- Refer to Figure5 UART pin definition connects the J16 interface of AP12276_M2 evaluation board to Host UART control interface.
- Connects an external antenna at SMA connector on the evaluation board.
- Note to the VDDIO voltage level should be the same as GPIO voltage level of Host CPU.

WiFi and Bluetooth software setup:

- Please follow up software guideline of Ampak official released.